channel region therebetween, a layer of gate dielectric material formed on a surface of the semiconductor substrate above the channel region and extending to at least partially overlap the source region [(120)] and the drain region, and a conductive gate [(104/106)] formed on the layer of gate dielectric material over the channel region, the method comprising:

forming a layer of first dielectric material [(108)] on the conductive gate [(104/106)] to define, in combination with the conductive gate, a stacked gate structure;

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forming a dielectric sidewall spacer structure [(110)] on sidewalls of the stacked gate structure and such that at least a first portion of the sidewall spacer structure is formed on gate dielectric materials that overlaps the drain region and at least a second portion of the sidewall spacer structure is formed on gate dielectric material that overlaps the source region [(120)];

forming a layer of second dielectric material [(112)] over the first dielectric material [(108)] and extending over the drain region such that the second dielectric material [(112)] is separated from the drain region by gate dielectric material and the first portion of the sidewall spacer structure [(110)], and extending over the source region [(120)] such that the second dielectric material [(112)] is separated from the source region [(120)] by gate dielectric material and the second portion of the sidewall spacer structure;

forming a contact trench [(116)] in the second dielectric material [(120)], the contact trench [(116)] having a first edge that is at least partially aligned over the conductive [floating] gate

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[(104/106)] and is at least partially defined by the second portion of the sidewall spacer structure, and a second edge that is aligned over the source region [(120)], the contact trench [(116)] defining an exposed surface of the source region [(120)];

forming a conductive lower capacitor plate [(114/118)] at least partially over the second dielectric material [(112)] and to <u>conformally</u> cover the first and second edges of the contact trench [(116)] and the exposed surface of the source region [(120)] <u>by forming a first layer of conductive material having a first thickness on the first and second edges of the contact trench and then forming a second layer of conductive material having a second thickness that is less than the first thickness on the first layer</u>;

forming a layer of capacitor dielectric material [(122)] over the lower capacitor plate [(114/118)]; and

forming a conductive upper capacitor plate [(124)] over the capacitor dielectric material [(122)].

Please add the following new claims:

-- ~~10.~~ A method as in claim ~~6~~ 1 and wherein the step of forming the conductive lower capacitor plate comprises depositing a first layer of polysilicon having a first thickness on the first and second edges of the contact trench, depositing a second layer of polysilicon having a second thickness that is less than the first thickness on the first layer, and patterning the first and second layers of polysilicon to define same lower capacitor plate.

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6 11. A method as in claim 6 and further comprising, after the step of forming the layer of second dielectric material, forming a thick conductive layer such that the step of forming the contact trench comprises forming the contact trench in the thick conductive layer and the layer of second dielectric. --

Please amend Claim 8 to read as follows:

3 8. (Amended) A method as in claim 1 wherein the conductive [floating] gate comprises a layer of first polysilicon having a layer of metal silicide formed thereon.

REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow:

In the September 20, 1996 Office Action in this application, the Examiner objected to the title of the application as being non-descriptive.

As indicated above, the title has been deleted in favor of a new title which clearly indicates that the application is directed to a method of fabricating a DRAM cell structure.

The Examiner has rejected claims 6-9 under 35 U.S.C. Section 112, second paragraph, as being indefinite, stating that in claim 6, line 41, "conductive floating gate" should be changed to "conductive gate."

As indicated above, claim 6 has been amended in accordance with the Examiner's suggestion.

The Examiner also stated that the reference characters included in the claims are not conventional.